CLAIMS

What is claimed is:

1. A process, comprising:

providing a device substrate having a dielectric layer thereon;

removing a portion of the dielectric layer to create an opening.

forming an interface layer within the opening;

forming a silver layer overlying the interface layer; and

annealing the substrate to form an intermetallic layer between the silver layer and the interface layer, in which the silver layer is in intimate contact with the intermetallic layer.

2. The process of claim 1, further comprising removing portion of the silver layer, intermetallic layer, and the interface layer overlying the dielectric layer to form a smooth surface.

3. The process of claim 1, wherein the interface layer comprises an adhesion layer and a diffusion barrier layer overlying the adhesion layer.

4. The process of claim 3, wherein the diffusion barrier layer comprises titanium nitride or tantalum nitride.

5. The process of claim 3, wherein the adhesion layer comprises titanium, tungsten, aluminum, or titanium nitride.

6. The process of claim 1, wherein the interface layer is formed using sputter deposition process.

7. The process of claim 1, wherein the silver layer is formed using sputter deposition process.

8. The process of claim 1, wherein the substrate is annealed at an ambient temperature of approximate 400 degree Celsius for a period of approximate one hour.

9. The process of claim 2, wherein the removing comprises a chemical-mechanical-polishing (CMP) process.

10. A process, comprising:

providing a device substrate;

forming an interface layer overlying the device substrate;

forming a silver layer overlying the interface layer;

annealing the substrate to form an intermetallic layer between the silver layer and the interface layer, in which the silver layer is in intimate contact with the intermetallic layer; and

forming a protection layer overlying the silver layer.

11. The process of claim 10, further comprising:

forming a patterned photoresist layer overlying the silver and interface layers;

etching the silver and the interface layers in alignment with the patterned photoresist layer, to form an interconnect; and

cleaning the silver layer, prior to annealing the substrate.

12. The process of claim 11, wherein forming a patterned photoresist layer is performed through an ultraviolet (UV) lithography process.

13. The process of claim 11, wherein the etching is performed through a dry etching process using oxygen (O_2) or carbon fluoride (CF_4) as source gas.

14. The process of claim 10, wherein the interface layer comprises an adhesion layer and a diffusion barrier layer overlying the adhesion layer.

15. The process of claim 14, wherein the diffusion barrier layer comprises titanium nitride or tantalum nitride.

16. The process of claim 14, wherein the adhesion layer comprises titanium, tungsten, or titanium nitride.

17. The process of claim 10, wherein the interface layer is formed using sputter deposition process.

18. The process of claim 10, wherein the silver layer is formed using sputter deposition process.

19. The process of claim 10, wherein the substrate is annealed at an ambient temperature of approximate 400 degree Celsius for a period of approximate one hour.

20. The process of claim 10, further comprising:

forming a dielectric layer overlying the protection layer; and

removing portion of the dielectric layer to form a smooth surface.

21. The process of claim 20, wherein the removing portion of the dielectric layer comprises a chemical-mechanical-polishing (CMP) process.

22. The process of claim 12, wherein the UV lithography process comprises:

placing a photoresist mask directly on the silver layer, without antireflective layers;

exposing the substrate under a UV light; and

developing the substrate.

23. The process of claim 10, wherein the protection layer comprises titanium (Ti), titanium nitride, or tungsten (W).

24. An interconnect structure, comprising:

a device substrate;

an interface layer overlying the device substrate;

a silver layer overlying the interface layer;

a protection layer overlying the silver layer; and

a dielectric layer overlying the protection layer.

25. The interconnect structure of claim 24, wherein the interface layer comprises an adhesion layer and a diffusion barrier layer overlying the adhesion layer.

26. The interconnect structure of claim 25, wherein the diffusion barrier layer comprises titanium nitride or tantalum nitride, and wherein the adhesion layer comprises titanium, titanium nitride, aluminum, or tungsten.

27. The interconnect structure of claim 24, wherein the protection layer comprises titanium, titanium nitride, or tungsten.

28. An interconnect structure, comprising:

a device substrate;

a dielectric layer overlying the device substrate, the dielectric layer having a cavity therein;

an interface layer overlying the dielectric layer, the interface layer having a thickness insufficient to completely fill the cavity; and

a silver layer overlying the interface layer, the silver layer having a thickness sufficient to completely fill the cavity.

29. The interconnect structure of claim 28, wherein the interface layer comprises an adhesion layer and a diffusion barrier layer overlying the adhesion layer.

30. The interconnect structure of claim 29, wherein the diffusion barrier layer comprises titanium nitride or tantalum nitride, and wherein the adhesion layer comprises titanium, titanium nitride, aluminum, or tungsten.